CURRICULUM PLAN 2024-2025
Even Semester: V, III, I
Dr. Rashmi Menon
Department of Physics

B.Sc.(H)-IIIrd year

Name of Paper and Code	Allocation of Lectures	Month-wise Schedule followed by the department
DSE 15: DIGITAL ELECTRONICS (32221502) -45 Periods		
Unit – I - Integrated circuits Integrated Circuits (Qualitative treatment only), active and passive components, discrete components, wafer, chip, advantages and drawbacks of ICs, scale of integration: SSI, MSI, LSI and VLSI (basic idea and definitions only), classification of ICs, examples of linear and digital lCs	2	5-Aug to 6-Aug
Unit – II - Digital circuits and Boolean algebra Difference between analog and digital circuits, binary number, decimal to binary and binary to decimal conversion, BCD, octal and hexadecimal numbers, AND, OR and NOT gates (realization using diodes and transistor), NAND and NOR gates as universal gates, XOR and XNOR gates and application as parity checkers De Morgan's theorems, Boolean laws, simplification of logic circuit using Boolean algebra, fundamental products, idea of minterms and maxterms, conversion of truth table into equivalent logic circuit by (1) Sum of Products method and (2) Karnaugh map simplification (up to four variables).	14	12-Aug to 10-Sept
Unit – III - Combinational Logic Circuits Data processing circuits: Multiplexers and its applications, de-multiplexers, decoders, encoders Arithmetic logic circuits: Express binary number in signed and unsigned form, 1's and 2's complement representation, binary addition, binary subtraction using 2's complement, half and full Adders, half and full subtractors, 4-bit binary adder/subtractor using 2's complement method.	9	23-Sept to 8-Oct

Unit – IV - Sequential Logic Circuits Flip Flops SR, D, and JK clocked (level and edge triggered) flip-flops, preset and clear operations, race-around conditions in JK flip-flop, master-slave JK flip-flop, conversion of one flip flop to another using an excitation table.	8	14-Oct to 29-Oct
Unit – V - Application of Sequential Logic Circuits Shift registers: Serial-in-Serial-out, Serial-in-Parallel-out, Parallel-in-Serial-out and Parallel in-Parallel-out Shift Registers (only up to 4 bits). Counters: Asynchronous counters, MOD-N synchronous counter designing using excitation table.	9	4-Nov to 19-Nov
Unit – VI – Timers IC 555: Pin -out diagram, block diagram and its applications as astable multivibrator and monostable multivibrator	3	25-Nov to 26-Nov